

LOGIC AND COMPUTER DESIGN FUNDAMENTALS

FIFTH EDITION

M. Morris Mano

California State University, Los Angeles

Charles R. Kime

University of Wisconsin, Madison

Tom Martin

Virginia Tech

PEARSON

Boston Columbus Indianapolis New York San Francisco Hoboken Amsterdam Cape Town Dubai London Madrid Milan Munich Paris Montreal Toronto Delhi Mexico City São Paulo Sydney Hong Kong Seoul Singapore Taipei Tokyo Vice President and Editorial Director, ECS: Marcia J. Horton

Acquisitions Editor: Julie Bai

Executive Marketing Manager: Tim Galligan

Marketing Assistant: Jon Bryant

Senior Managing Editor: Scott Disanno Production Project Manager: Greg Dulles

Program Manager: Joanne Manning

Global HE Director of Vendor Sourcing and

Procurement: Diane Hynes
Director of Operations: Nick S

Director of Operations: Nick Sklitsis

Operations Specialist: *Maura Zaldivar-Garcia* Cover Designer: *Black Horse Designs*

Manager, Rights and Permissions: *Rachel Youdelman* Associate Project Manager, Rights and Permissions:

Timothy Nicholls

Full-Service Project Management: Shylaja Gattupalli,

Jouve India

Composition: *Jouve India* Printer/Binder: *Edwards Brothers*

Cover Printer: Phoenix Color/Hagerstown

Typeface: 10/12 Times Ten LT Std

Copyright © 2015, 2008, 2004 by Pearson Higher Education, Inc., Hoboken, NJ 07030. All rights reserved. Manufactured in the United States of America. This publication is protected by Copyright and permissions should be obtained from the publisher prior to any prohibited reproduction, storage in a retrieval system, or transmission in any form or by any means, electronic, mechanical, photocopying, recording, or likewise. To obtain permission(s) to use materials from this work, please submit a written request to Pearson Higher Education, Permissions Department, 221 River Street, Hoboken, NJ 07030.

Many of the designations by manufacturers and seller to distinguish their products are claimed as trademarks. Where those designations appear in this book, and the publisher was aware of a trademark claim, the designations have been printed in initial caps or all caps.

The author and publisher of this book have used their best efforts in preparing this book. These efforts include the development, research, and testing of theories and programs to determine their effectiveness. The author and publisher make no warranty of any kind, expressed or implied, with regard to these programs or the documentation contained in this book. The author and publisher shall not be liable in any event for incidental or consequential damages with, or arising out of, the furnishing, performance, or use of these programs.

Library of Congress Cataloging-in-Publication Data

Mano, M. Morris, 1927-

Logic and computer design fundamentals / Morris Mano, California State University, Los Angeles; Charles R. Kime, University of Wisconsin, Madison; Tom Martin, Blacksburg, Virginia. — Fifth Edition.

ISBN 978-0-13-376063-7 — ISBN 0-13-376063-4

1. Electronic digital computers—Circuits. 2. Logic circuits. 3. Logic design. I. Kime, Charles R. II. Martin, Tom, 1969- III. Title.

TK7888.4.M36 2014

621.39'2—dc23 2014047146

10 9 8 7 6 5 4 3 2 1



ISBN-10: 0-13-376063-4 ISBN-13: 978-0-13-376063-7

Contents

Preface ☐ Chapte	er 1 3	xii
Digital S	Systems and Information	3
1-1	Information Representation	4
	The Digital Computer	6
	Beyond the Computer	7
	More on the Generic Computer	10
1-2	Abstraction Layers in Computer Systems Design	12
	An Overview of the Digital Design Process	14
1-3	Number Systems	15
	Binary Numbers	17
	Octal and Hexadecimal Numbers	18
	Number Ranges	20
1-4	Arithmetic Operations	20
	Conversion from Decimal to Other Bases	23
1-5	Decimal Codes	25
1- 6	Alphanumeric Codes	26
	ASCII Character Code	26
	Parity Bit	29
1-7	Gray Codes	30
1-8	Chapter Summary	32
	References	33
	Problems	33
□ Chapte	er 2 37	
Combina	tional Logic Circuits	37
2-1	Binary Logic and Gates	38
	Binary Logic	38
	Logic Gates	40
	HDL Representations of Gates	44

□ iii

iv 🗆 (Contents	
2-2	Boolean Algebra	4
	Basic Identities of Boolean Algebra	4
	Algebraic Manipulation	5
	Complement of a Function	5
2-3	Standard Forms	5.
	Minterms and Maxterms	5.
	Sum of Products	5
	Product of Sums	6
2-4	Two-Level Circuit Optimization	6
	Cost Criteria	6
	Map Structures	6
	Two-Variable Maps	6.
	Three-Variable Maps	6
2-5	Map Manipulation	7
	Essential Prime Implicants	7
	Nonessential Prime Implicants	7.
	Product-of-Sums Optimization	7.
2.6	Don't-Care Conditions	7.
2-6	Exclusive-Or Operator and Gates	7
2.7	Odd Function	7.
2-7	Gate Propagation Delay HDLs Overview	8
2-8		8:
2-9	Logic Synthesis	8
2 - 9 2 - 10	HDL Representations—VHDL	9.
2 - 10 2 - 11	HDL Representations—Verilog	10
2-11	Chapter Summary References	10
	Problems	10.
	Fromenis	10.
□ Chapter	· 3 113	
	ional Logic Design	113
3-1	Beginning Hierarchical Design	11-
3-2	Technology Mapping	11
3-3	Combinational Functional Blocks	12
3-4	Rudimentary Logic Functions	12
	Value-Fixing, Transferring, and Inverting	12
	Multiple-Bit Functions	12
	Enabling	12
3-5	Decoding	12
	Decoder and Enabling Combinations	13:
2.6	Decoder-Based Combinational Circuits	13.
3-6	Encoding	13
	Priority Encoder	13
	Encoder Expansion	13

		Contents	L V
3-7	Selecting		140
3-7	Multiplexers		140
	Multiplexer-Based Combinational Circuits		150
3-8	Iterative Combinational Circuits		155
3-9	Binary Adders		157
	Half Adder		157
	Full Adder		158
	Binary Ripple Carry Adder		159
3-10	Binary Subtraction		161
	Complements		162
	Subtraction Using 2s Complement		164
3-11	Binary Adder-Subtractors		165
	Signed Binary Numbers		166
	Signed Binary Addition and Subtraction		168
	Overflow		170
	HDL Models of Adders		172
	Behavioral Description		174
3-12	Other Arithmetic Functions		177
	Contraction		178
	Incrementing		179
	Decrementing		180
	Multiplication by Constants		180
	Division by Constants		182
2.12	Zero Fill and Extension		182
3-13	Chapter Summary		183
	References		183
	Problems		184
□ Chapter 4	197		
Sequential (Circuits		197
4- 1	Sequential Circuit Definitions		198
4-2	Latches		201
	SR and \overline{SR} Latches		201
	D Latch		204
4-3	Flip-Flops		204
	Edge-Triggered Flip-Flop		206
	Standard Graphics Symbols		207
	Direct Inputs		209
4-4	Sequential Circuit Analysis		210
	Input Equations		210
	State Table		211
	State Diagram		213
	Sequential Circuit Simulation		216
4-5	Sequential Circuit Design		218

vi 🔲 Coi	ntents	
	Design Procedure	218
	Finding State Diagrams and State Tables	219
	State Assignment	220
	Designing with D Flip-Flops	22
	Designing with Unused States	230
	Verification	232
4-6	State-Machine Diagrams and Applications	234
	State-Machine Diagram Model	236
	Constraints on Input Conditions	238
	Design Applications Using State-Machine Diagrams	240
4-7	HDL Representation for Sequential Circuits—VHDL	248
4-8	HDL Representation for Sequential Circuits—Verilog	25
4-9	Flip-Flop Timing	266
4-10	Sequential Circuit Timing	26
4-11	Asynchronous Interactions	270
4-12	Synchronization and Metastability	27.
4-13	Synchronous Circuit Pitfalls	27
4-14	Chapter Summary	278
	References	279
	Problems	280
□ Chapter 5	295	
Digital Hai	RDWARE IMPLEMENTATION	295
5-1	The Design Space	29:
	Integrated Circuits	295
	CMOS Circuit Technology	296
	Technology Parameters	302
5-2	Programmable Implementation Technologies	304
	Read-Only Memory	306
	Programmable Logic Array	308
	Programmable Array Logic Devices	31.
	Field Programmable Gate Array	313
5-3	Chapter Summary	318
	References	318
	Problems	318
□ Chapter 6	323	
Registers a	nd Register Transfers	323
6-1	Registers and Load Enable	324
	Register with Parallel Load	325
6-2	Register Transfers	32
6-3	Register Transfer Operations	329
6-4	Register Transfers in VHDL and Verilog	333

		Contents	vii
- -			
6-5	Microoperations		332
	Arithmetic Microoperations		333
	Logic Microoperations		335
	Shift Microoperations		337
6-6	Microoperations on a Single Register		337
	Multiplexer-Based Transfers		338
	Shift Registers		340
	Ripple Counter		345
	Synchronous Binary Counters		347
	Other Counters		351
6-7	Register-Cell Design		354
6-8	Multiplexer and Bus-Based Transfers for		2.50
	Multiple Registers		359
	High-Impedance Outputs		361
6.0	Three-State Bus		363
6-9	Serial Transfer and Microoperations		364
6.10	Serial Addition		365
6-10	Control of Register Transfers		367
~ 4.4	Design Procedure		368
6-11	HDL Representation for Shift Registers		
c 10	and Counters—VHDL		384
6-12	HDL Representation for Shift Registers		
6.40	and Counters—Verilog		386
6-13	Microprogrammed Control		388
6-14	Chapter Summary		390
	References		391
	Problems		391
	402		
□ Chapter 7	403		
Memory Bas	ICS		403
7- 1	Memory Definitions		403
7- 2	Random-Access Memory		404
	Write and Read Operations		406
	Timing Waveforms		407
	Properties of Memory		409
7 - 3	SRAM Integrated Circuits		409
	Coincident Selection		411
7 - 4	Array of SRAM ICs		415
7 - 5	DRAM ICs		418
	DRAM Cell		419
	DRAM Bit Slice		420
7 - 6	DRAM Types		424
. •	Synchronous DRAM (SDRAM)		426
	Double-Data-Rate SDRAM (DDR SDRAM)		428
	(

viii 🗆 (Contents	
7-7 7-8	RAMBUS® DRAM (RDRAM) Arrays of Dynamic RAM ICs Chapter Summary References	429 430 430 431
	Problems	431
□ Chapter 8	3 433	
Computer I	Design Basics	433
8-1	Introduction	434
8-2	Datapaths	434
8-3	The Arithmetic/Logic Unit	437
	Arithmetic Circuit	437
	Logic Circuit	44(
	Arithmetic/Logic Unit	442
8-4	The Shifter	443
0.1	Barrel Shifter	444
8-5	Datapath Representation	445
8 - 6	The Control Word	447
8 - 7	A Simple Computer Architecture	453
0-7	Instruction Set Architecture	453
	Storage Resources	454
	Instruction Formats	455
0.0	Instruction Specifications	457
8-8	Single-Cycle Hardwired Control	460
	Instruction Decoder	461
	Sample Instructions and Program	463
	Single-Cycle Computer Issues	466
8-9	Multiple-Cycle Hardwired Control	467
	Sequential Control Design	471
8-10	Chapter Summary	476
	References	478
	Problems	478
□ Chapter 9	485	
Instruction	N SET ARCHITECTURE	485
9-1	Computer Architecture Concepts	485
	Basic Computer Operation Cycle	487
	Register Set	487
9-2	Operand Addressing	488
<i>)</i> <u>-</u>	Three-Address Instructions	489
	Two-Address Instructions	489
	One-Address Instructions	490
	One-Audress monucuons	490

		Contents	ix
	Zero-Address Instructions		490
	Addressing Architectures		491
9-3	Addressing Modes		494
	Implied Mode		495
	Immediate Mode		495
	Register and Register-Indirect Modes		496
	Direct Addressing Mode		496
	Indirect Addressing Mode		497
	Relative Addressing Mode		498
	Indexed Addressing Mode		499
	Summary of Addressing Modes		500
9-4	Instruction Set Architectures		501
9-5	Data-Transfer Instructions		502
	Stack Instructions		502
	Independent versus Memory-Mapped I/O		504
9-6	Data-Manipulation Instructions		505
, 0	Arithmetic Instructions		505
	Logical and Bit-Manipulation Instructions		506
	Shift Instructions		508
9-7	Floating-Point Computations		509
) - 1	Arithmetic Operations		510
	Biased Exponent		511
	Standard Operand Format		512
9-8	Program Control Instructions		514
9- 0	Conditional Branch Instructions		515
	Procedure Call and Return Instructions		517
9-9			519
9 - 9	Program Interrupt		520
	Types of Interrupts Processing Enterrupts		521
9-10	Processing External Interrupts Chapter Supports		521
9-10	Chapter Summary		
	References		523
	Problems		523
□ Chapter 10	531		
RISC AND CISC	CENTRAL PROCESSING UNITS		531
10-1	Pipelined Datapath		532
	Execution of Pipeline Microoperations		536
10-2	Pipelined Control		537
	Pipeline Programming and Performance		539
10-3	The Reduced Instruction Set Computer		541
	Instruction Set Architecture		541
	Addressing Modes		544
	Datapath Organization		545
	Control Organization		548

x Conte	nts	
	Data Hazards	550
	Control Hazards	557
10-4	The Complex Instruction Set Computer	561
	ISA Modifications	563
	Datapath Modifications	564
	Control Unit Modifications	566
	Microprogrammed Control	567
	Microprograms for Complex Instructions	569
10-5	More on Design	572
	Advanced CPU Concepts	573
	Recent Architectural Innovations	576
10-6	Chapter Summary	579
	References	580
	Problems	581
□ Chapter 11	585	
INPUT—OUTP	ut and Communication	585
11-1	Computer I/O	585
11-2	Sample Peripherals	586
	Keyboard	586
	Hard Drive	587
	Liquid Crystal Display Screen	589
	I/O Transfer Rates	592
11-3	I/O Interfaces	592
	I/O Bus and Interface Unit	593
	Example of I/O Interface	594
	Strobing	595
	Handshaking	597
11-4	Serial Communication	598
	Synchronous Transmission	599
	The Keyboard Revisited	600
	A Packet-Based Serial I/O Bus	601
11-5	Modes of Transfer	604
	Example of Program-Controlled Transfer	605
	Interrupt-Initiated Transfer	606
11-6	Priority Interrupt	608
	Daisy Chain Priority	608
	Parallel Priority Hardware	610
11-7	Direct Memory Access	611
	DMA Controller	612
	DMA Transfer	614
11-8	Chapter Summary	615
	References	615
	Problems	616

□ Chapter 12 **619**

Memory S	YSTEMS	619
12-1	Memory Hierarchy	619
12-2	Locality of Reference	622
12-3	Cache Memory	624
	Cache Mappings	626
	Line Size	631
	Cache Loading	632
	Write Methods	633
	Integration of Concepts	634
	Instruction and Data Caches	636
	Multiple-Level Caches	637
12-4	Virtual Memory	637
	Page Tables	639
	Translation Lookaside Buffer	641
	Virtual Memory and Cache	643
12-5	Chapter Summary	643
	References	644
	Problems	644
Index		648